D0 Muon Scintillator Electronics Readout Controller (SRC) Specification

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Revised:

1. Introduction

Figure 1-1 is a block diagram of the overall Muon Scintillator Front End System consisting of 6500 channels of Photomultiplier Tube (PMT) signals input to approximately 137 Scintillator Front End (SFE) modules, each with 48 channels. The SFE modules are housed in sixteen (16) 9U x 280 mm VME crates located on the D0 Platform and in various places on the detector. Each crate contains a 680xx processor, a Scintillator Readout Controller (SRC) module, a Scintillator LED Pulser (SLP) module and approximately 10 SFE modules. The SFE modules accept and process event data from all crossings and provide an event data buffer for Level 1 accepted events. The SRC collects and further processes Level 1 accepted event data from all SFEs in the crate. The SLP is a test module that is used to stimulate the scintillator counters producing PMT signals to the SFEs for testing purposes.

The Proportional Drift Tube (PDT) electronics is another D0 Muon subsystem for which the SRC has a parallel roll to the PDT Control Board (CB). The design of the SRC is based on the CB design and will duplicate it wherever possible. As a result, much of this document is copied directly from the CB specification. Differences between the CB and SRC designs will be discussed in more detail.

Level 1 (L1) trigger data corresponding to HIT channels is sent directly from each SFE to the Muon Trigger system for each 132 ns crossing interval via a 1 Gbit/s serial link. It is expected that the scintillator system will have a 1% occupancy which implies that on average only one channel will be HIT every other crossing. Event data is processed and temporally stored for each crossing for as long as 4.7 μs while the L1 trigger decision is made. The Muon Trigger system processes the scintillator trigger data along with that of other Muon subsystems and sends its decision to the Trigger Framework (TFW) which processes trigger data from the entire detector. The SRC module receives timing and trigger information about the L1 accepted events from the Trigger Framework via the Serial Command Link (SCL) and passes it on to the SFE modules. Identification of accepted events temporarily being stored in the SFE is determined by the arrival time of an L1 accept signal

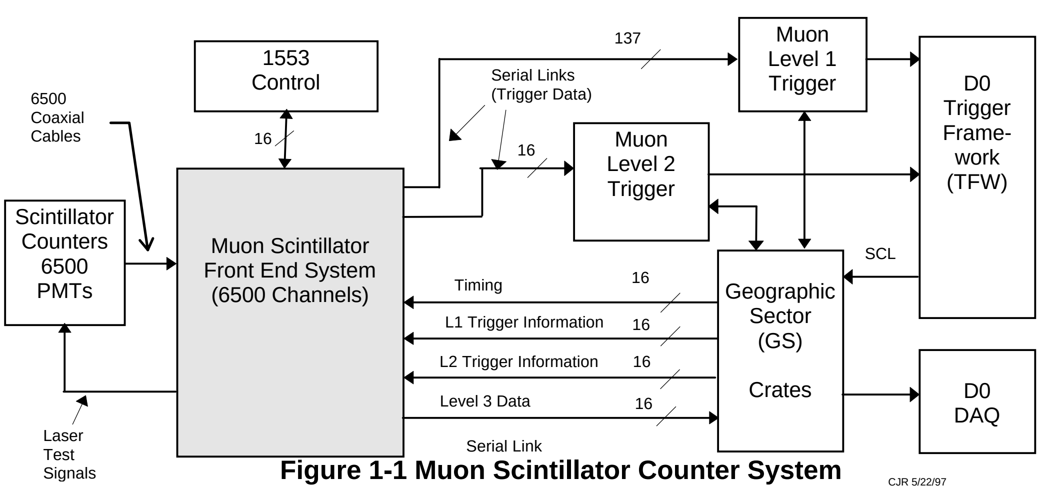


Figure 1-1 Muon Scintillator Counter System

to within one crossing interval. Upon receipt of the L1 Accept, data from the accepted event is transferred to one of 16 buffer pages of a dual port memory, comprising the SFE L1 Buffer.

Transfer of event data from the SFEs to the SRC is initiated by the SRC immediately following an L1 Accept. The SRC addresses each SFE module in the crate which then outputs its data to one of 16 pages of a dual port memory on the SRC. The dual port on the SRC then serves as an L1 Buffer for the entire crate. After all modules have been read out, the Digital Signal Processor (DSP) on the SRC is notified that the event is ready for readout. The DSP reads, reformats, and transfers selected event data from the SRC L1 Buffer to a Level 2 (L2) trigger data queue for output to the Muon L2 Trigger System via a 160 Mbit/s serial link. The DSP awaits the L2 trigger decision from the Trigger Framework and reformats and transfers L2 accepted events to the Level 3 data queue for output to the MRC via an additional 160 Mbit/s serial link.

2. General Description

Functions of the SRC Module include:

1) Read L1 accepted event data from the SFE L1 buffer of each SFE in the crate into a dual port memory on the SRC having 16 pages of event buffering for the entire crate.

2) Reformat and output L1 accepted event data to the L2 Trigger system via a 160 Mbit/s serial link.

3) Reformat and output accepted L2 event data to the MRC via a 160 Mbit/s serial link.

4) Manage event data transfers based upon receipt of L1 Accept, L2 Accept, and L2 Reject trigger decisions

5) Accept beam timing signals from MRC and provide a means to position timing signals to event data signals at the SFE.

6) Provide 1553 interface to download the 680xx crate processor.

7) Implement programmable Test Pulse generator.

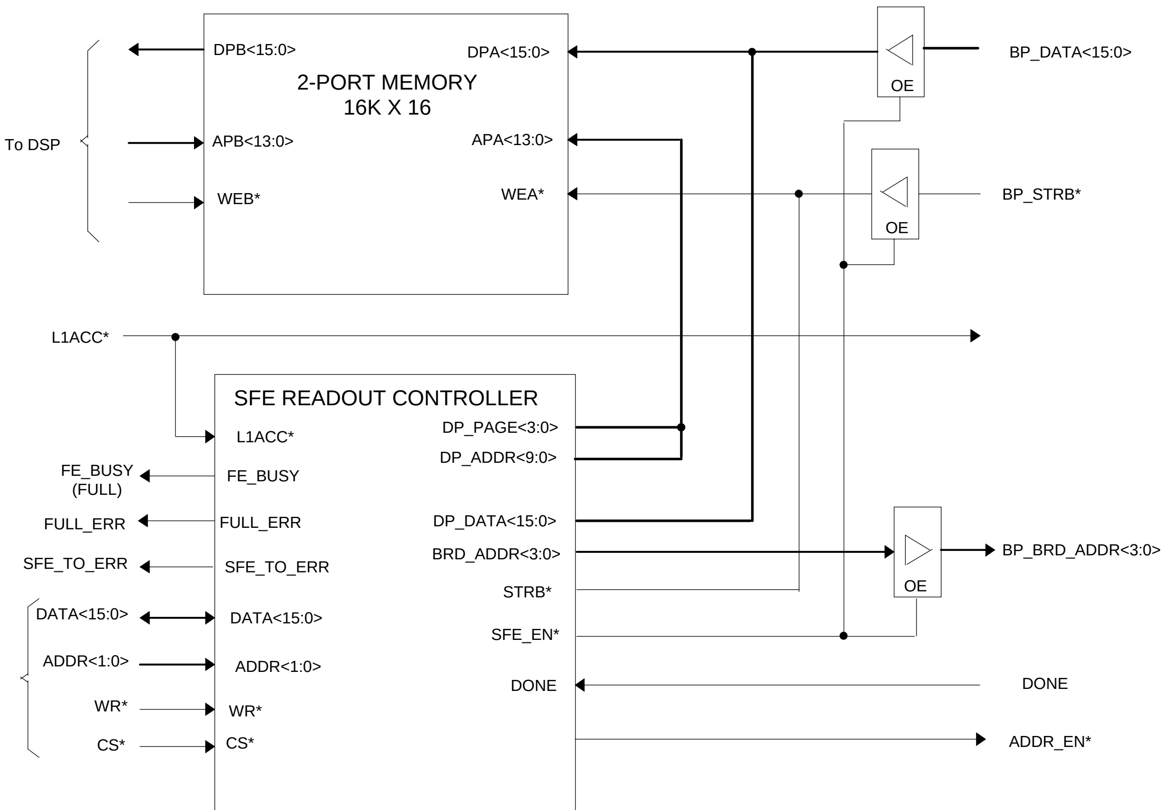
Trigger decisions are sent to the SRC by means of a 50 pair ribbon cable running from the MRC in the MCH to the collision hall. Peaking networks are fitted to each signal pair to increase the effective bandwidth of the cable, since the intrinsic bandwidth of this cable is less than 7MHz. To keep E.M.I. radiation to a minimum, current mode transmission is used. Encoded timing information is sent on one section of a four conductor ribbon coaxial cable also running from the MRC to the platform. The other conductors are used for L2 trigger data, L3 data, and a 53MHz clock. To enforce a balance between center conductor and shield currents, and thus reduce E.M.I., transformer coupling is used. This has the additional feature of breaking any ground loops between the MCH and the platform.

An on-board timing generator can delay all the arriving timing signals a programmable amount as a means of synchronizing the operation of all SFEs in the crate. For test pulsing, a programmable test pulse generator is fitted.

The SRC uses a Analog Devices 21Csp-01 DSP to control the data acquisition process and has a VME slave interface for control and status read back of various downloaded parameters via the 680xx. Since there is no direct remote access available for the crates 680xx processor, a remote access interface is implemented with a 1553 interface on the SRC. The 1553 interface interrupts the 680xx which then fetches the download information via the SRC's VME slave interface.

3. SFE Readout

One of the major differences between the Proportional Drift tube and Scintillator systems is the readout of their respective front end modules. The SRC has a 16 bit by 16K dual port memory organized in 16 pages for the purpose of buffering 16 events with up to 100% occupancy of L1 accepted events for the entire crate. In essence, it is an L1 Buffer for the entire crate. Transfer of event data from the SFEs to the SRC begins immediately following an L1 Accept and is entirely



CONTROL & STATUS REGISTERS

CSR0 Read/Write		
D<15:0>	SFE_MASK<15:0>	Bit map of which SFEs to read out
CSR1 Write		
D<7:0>	TO_SET<7:0>	Timeout Setting 1 LSB = 76 ns
D<15:8>	Not Used	
CSR1 Read		
D<7:0>	TO_SET<7:0>	Timeout Setting 1 LSB = 76 ns
D<11:8>	TO_ERR_ADR<3:0>	Address of first SFE to cause TO error
D12	SFE_TO_ERR	SFE Timeout Error
D13	FULL_ERR	Buffer page has been over written
D<15:14>	Not Used	
CSR2 Write Not Used		
CSR2 Read		
D<15:0>	PG_FULL	Bit map of buffer pages in use
CSR3 Write Not Used		
CSR3 Read		
D<7:0>	L1_COUNT<3:0>	Rolling Counter of L1 Accepts
D<11:8>	DP_PAGE<3:0>	Current or next page 2-Port pointer
D<15:9>	Not Used	

Figure 3-1 SFE Readout Interface

controlled by the SFE Readout Control implemented in an Alter Flex 10K10 PLD. Figure 3-1 shows interconnections between the controller and the dual port along with the definition of various control parameters.

Figure 3-2 shows the format of the event readout as it resides in the dual port.

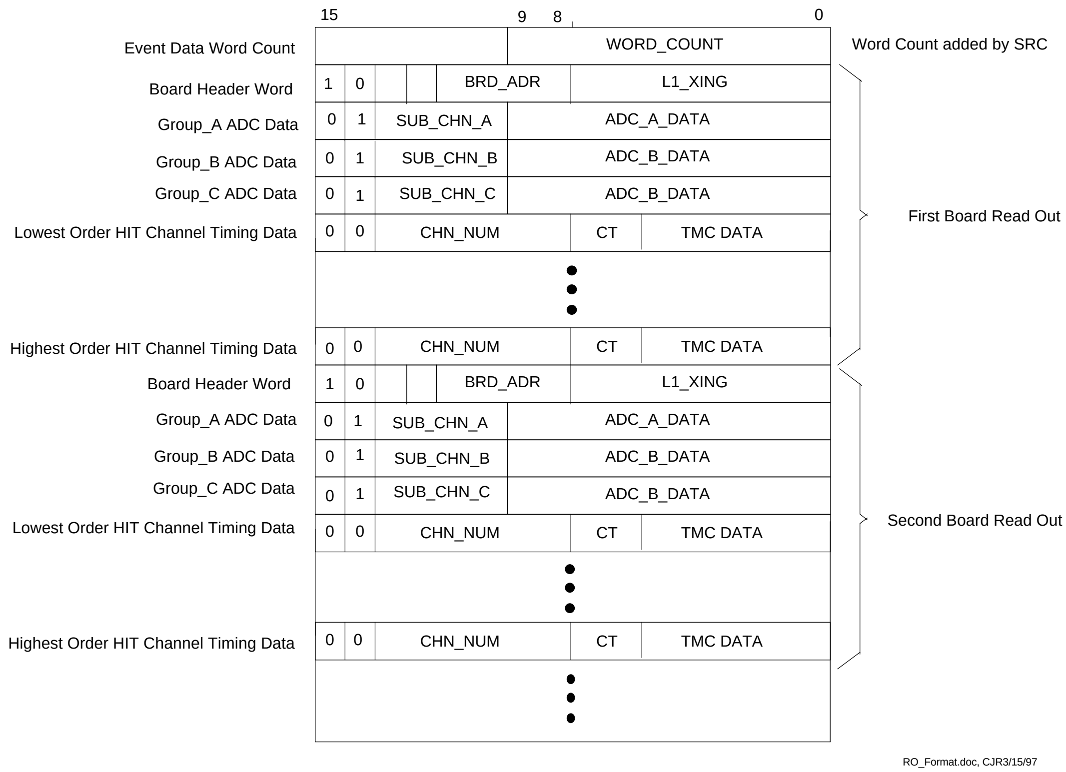


Figure 3-2 Event Readout Format

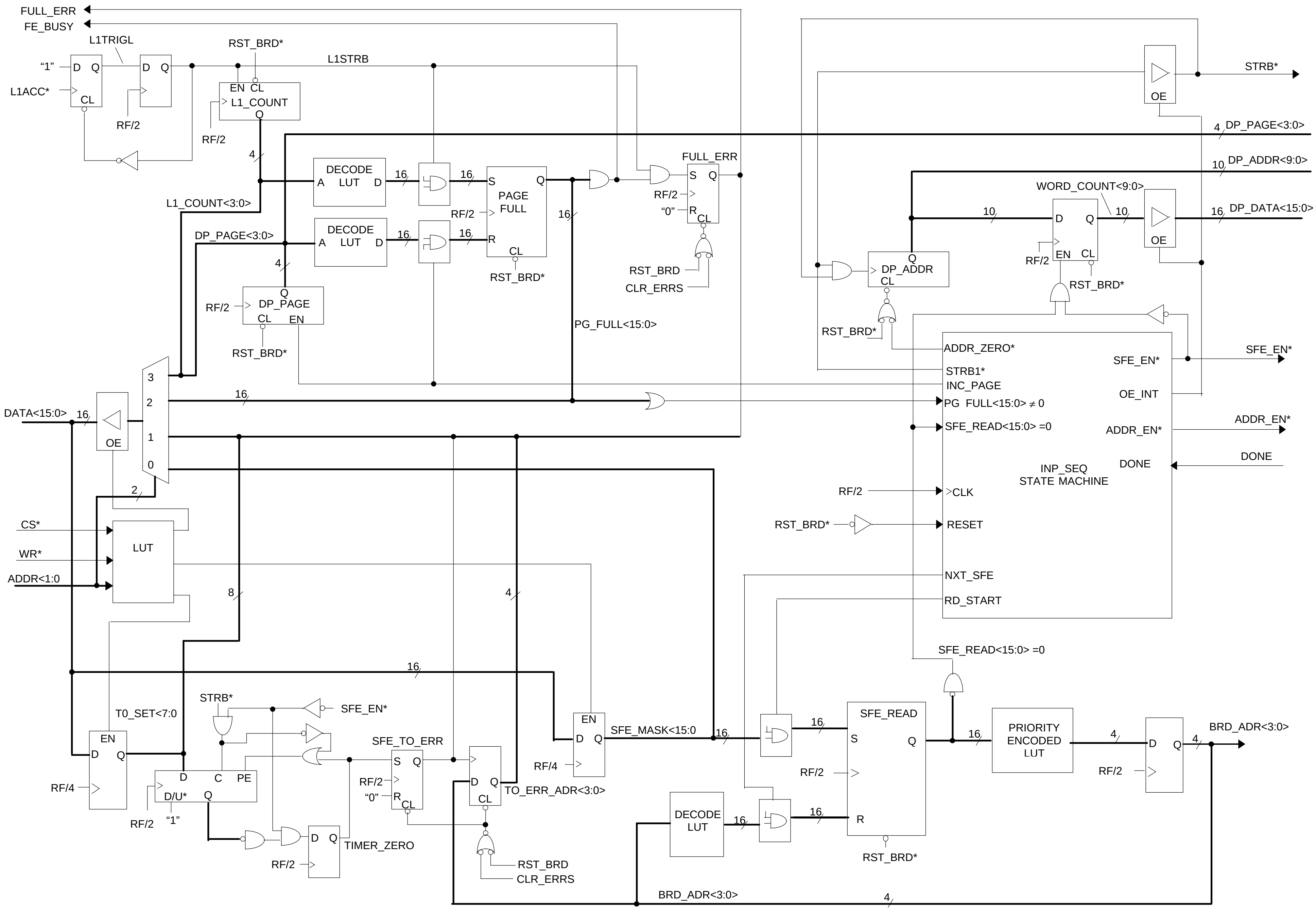


Figure 3-3 SFE Readout Controller Functional Schematic

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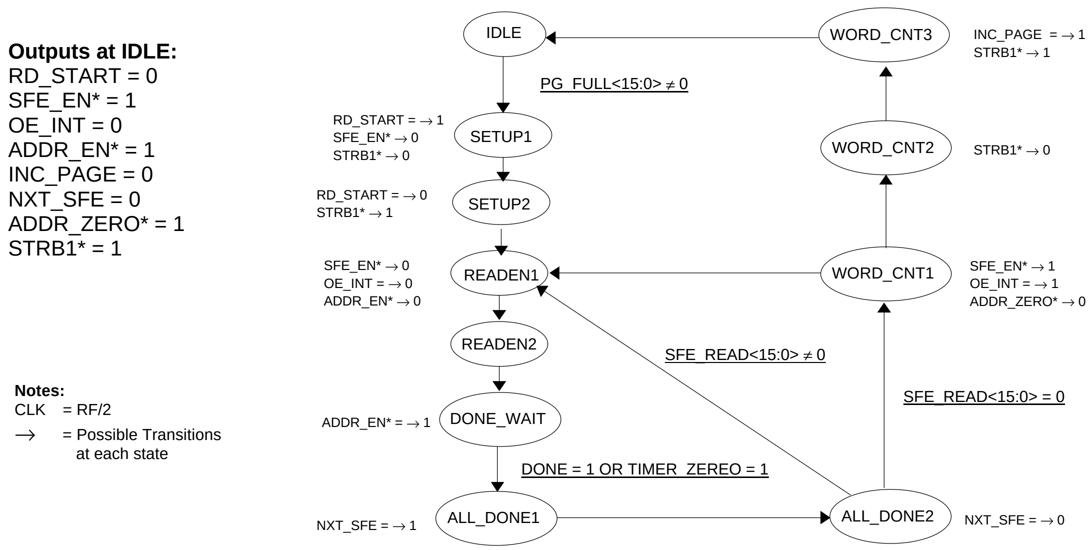

Figure 3-4 SFE Readout Controller State Machine

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Figure 3-3 is a function schematic of the SFE Readout Controller. Overall control of the readout is provided by the state machine, INP_SEQ, whose state diagram is shown in Figure 3-4. L1ACC increments a counter called L1_COUNT and another counter called DP_PAGE is incremented at the end of the readout of each event. DP_PAGE points to the current or next buffer page to be read out. Each counter is decoded to appropriately set and reset a corresponding bit in a 16 bit register called PAGE FULL whose output called PG_FULL being non zero initiates the readout process. A 16 bit readout mask (SFE_MASK<15:0>) is downloaded to the controller and determines which SFE modules are to be read out. The SFE board address is encoded and output (BRD_ADDR<3:0>) to the J3 data bus along with ADDR_EN*. An address lock between the SRC and an SFE is established by the requirement that the SFE begins to outputs its data within a programmable timeout period (TO_SET<7:0>). Data is transmitted along a bussed J3 backplane using ABT technology TTL drivers with an accompanying data strobe, STRB* at a 13 MHz (RF/4) rate. Data is input directly to the dual port with addressing controlled by the readout controller which also keeps track of the word count. Each SFE sends DONE when all its data has been read out. The controller addresses successive SFEs until all specified SFEs have been readout at which time the controller writes the total data word count at the zero location of the corresponding buffer page. The controller then interrupts the DSP to signify that the readout is done.

Expected readout times for a crate with 10 SFEs at various occupancies are:

- 1 % Occupancy - 7.1 μs
- 10% Occupancy - 12.1 μs
- 100 % Occupancy - 47.6 μs

The readout controller asserts FE_BUSY whenever the all 16 L1 buffer pages are in use (PG_FULL = FFFFh). If an L1ACC occurs under this condition, the controller asserts FULL_ERR to signify that the readout controller has detected an error. This information will be available through VME for diagnostic purposes only since the DSP will also no of these conditions and determine the appropriate action to take when they occur.

4. DAQ Control Signals

The signals arriving from the Trigger Framework (TFW) include INIT, L1 Accept, L2 Accept, L2 Reject and eight bits of crossing number associated with a particular trigger decision. The timing of L1 Accept determines which event is accepted and hence transferred to the L1 Buffer on each SFE and is the highest priority interrupt of the DSP. L2 accept and reject are OR'ed to form the next highest priority DSP interrupt. The incoming crossing number is latched in the case of L1 Accepts to be read by the DSP. For crossing number for L2 decisions is written into a crossing number FIFO for later reading by the processor during its trigger decision interrupt service routine. These crossing numbers are compared to on-board crossing and turn counters as a check for proper event synchronization. The signals BUSY 1, BUSY 2, ERROR 1, and ERROR 2 are returned to the TFW by way of the MRC when the appropriate condition occurs.

5. Timing decoder

Timing signals must be recovered from the encoded serial stream. A commercially available cable equalizer and clock recovery chip (National CLC014, CLC016) are used to restore the attenuated signal to PECL logic levels and separate the serial data from the 106MHz clock used for encoding. This signal clocks a state machine realized with a 7ns 22V10 PAL chip which de-serializes the data into First Crossing, GAP, and Sync Gap and divides the 106MHz down to 53MHz. For the SFEs, GAP has no relevance and is not used. By sending clock and data through the same drivers, receivers and cable, their phase relationship is constant. The RF (53MHz) reference clock which is coming from the TFW SCL board is de-jittered by means of a CY7B991. The RF reference is used to re-phase the RF/7 crossing interval clock before being sent to the SFEs where it is used as the clock for TMCs. These chips allow for a jumper selectable phase adjustment of 9 steps of about 1.2 ns each.

6. VME Interface

The peripherals under VME control include:

6.1. Serial Ports:

One channel of an AM85C30 dual SCC is used as a local RS-232 terminal port and the second channel is setup to use FM encoding with a special double speed clocking mode to attain a speed of 2.5 Mbits/s on a single line for transmit and receive line running to and from the movable counting house. The SRCs do not require a high speed connection, but in the interests of consistency, this SCC is used in all Muon sub-systems, including the L1 trigger system, where the bandwidth is useful for downloading large tables.

6.2. Test Pulse Generator

Separate turn and crossing counters are implemented to allow the adjustment of the timing and repetition rate of test pulses. A 16 bit counter counts turns while a crossing counter counts at the 7 MHz rate and a vernier modulo seven counter runs at 53MHz. A test pulse can be generated at a resolution of 2 ns anywhere within a turn every N turns where N is the prescaled value loaded into the turn counter. To a resolution of 19 ns, counters determine the pulser timing. The finest steps are adjusted by means of a 10 tap 2ns per tap delay line.

6.3. Timing Generator

It is the responsibility of the TFW to send beam timing information early enough so that the detector with the greatest cable delay will still get the timing information ahead of the actual beam crossings. It is the responsibility of each front-end system to trim the timing on these incoming signals so that they match the local timing of the interactions. This timing depends on many factors: cable lengths, electronics delays, physical distance from the interaction region etc.

The length of the pipeline delays must be adjusted to match exactly the sum of the propagation delays and the L1 trigger decision time. This cannot be known a priori to the necessary precision and must be trimmed based on measured times. The test pulse generator can be used to measure the trigger decision time, and thus the value of the pipeline delay. Beam data is used to align the timing sequence to the interactions. For this adjustment, the beam and pipeline delays must be moved together to preserve a fixed relationship between the data emerging from the pipeline and the time of arrival of L1 Accept.

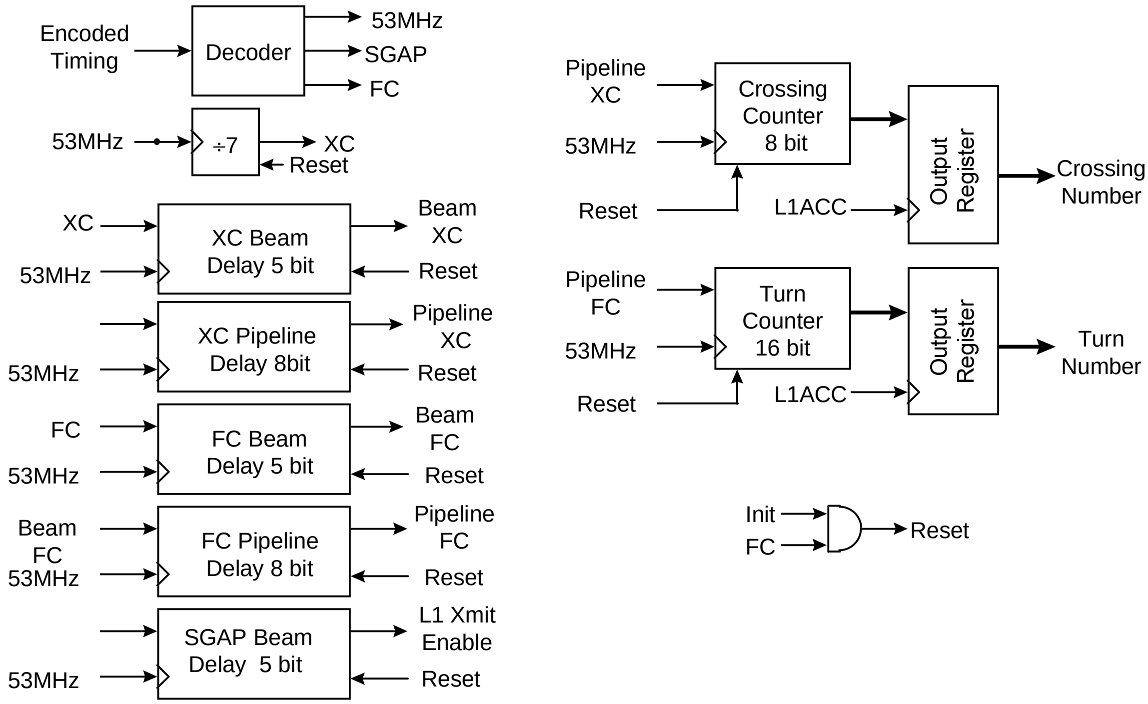

Figure 6-1 Timing Control

7. DSP Controller

The DSP is used to control the overall data acquisition process. To that end there are interrupts for trigger decisions and the SFE readout done of Level 1 accepted events. The processor chosen is an AD21Csp-01 fixed point DSP processor running at 50MHz. This device is sufficiently powerful to perform almost all data taking (with the exception of SFE readout) under software control, thus affording a degree of flexibility in the face of changing requirements. It also has the effect of shifting the operational burden from hardware to software. A block diagram of the DSP control logic is shown in Figure 7-1.

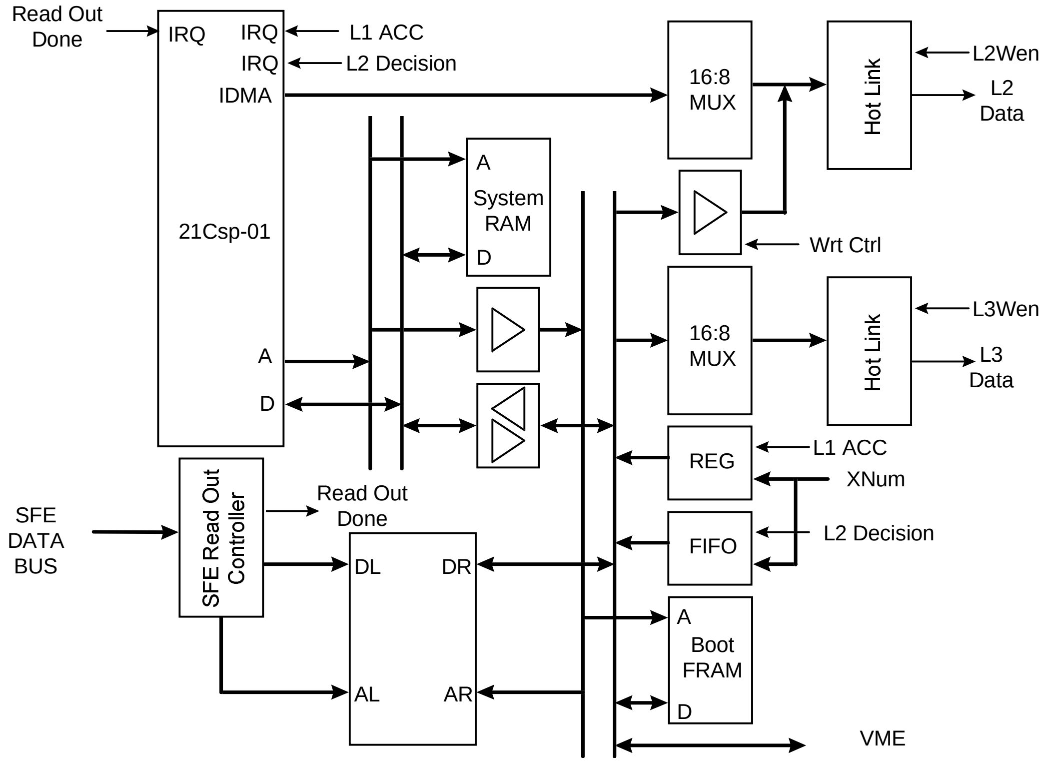

Figure 7-1 DSP Control Logic Interface

7.1. Heartbeat

The system reset chip will issue a processor reset if it does not receive a heartbeat input within 300ms. This will obviate the need for remote reset in the event of a software hang. A flag out pin on the processor is attached to the heartbeat pin of the reset chip. There are a number of ways that a heartbeat can be issued. A internal periodic interrupt from the processor's on-chip timer is one possibility.

7.2. Local Triggering

In order to facilitate local test triggers, the Trigger OR output of each SFE is wire ORed on the data bus. This signal is input to a local delay simulating the timing of the TFW. When this delay is set correctly, there will be no need to modify the timing generator settings when switching between local triggers and the TFW. A Trig IN LEMO is also provided for something like a local scintillator coincidence to be able to trigger a data acquisition routine. Alternatively, the Trig IN could come from a local multi-layer coincidence trigger generated by special tables loaded into the L1 trigger system.

7.3. Trigger Information Registers

In addition to the crossing number coming from the TFW, on board crossing and turn counters are clocked by appropriately phased copies of the beam orbit timing signals. The processor can immediately check the internal and external crossing numbers for consistency, but because the bandwidth required to ship turn numbers from the MCH along with the triggers is prohibitively large, the internally generated turn number is sent to the MCH as part of the L3 data block and compared to the TFW generated turn number there.

7.4. L2 Data Transmission

Each L1 accept begins the readout process. Once the readout controller has finished writing an event into the Dual Port RAM, the processor must reformat and truncate the data prior to sending it to L2, and arbitrary units are normalized to standard units. The IDMA port is used to send L2 data without processor intervention, however, control data must be sent. It is for this reason that there is an alternate path to the L2 serial transmitter for the specific purpose of sending the block begin and block end control characters required by the L2 data receiver card to detect event boundaries.

7.5. L3 Data Transmission

The transmission of L3 data is under direct processor control and is presumably a low priority background process, since the expected L3 event rate is 1KHz. No alternate path is needed for control characters in this case. The test and transparent modes of both Hot Link interfaces are controlled by the DSP.

Appendix:

Processor:
DSP - Analog Devices ADSP21Csp-01 operating at 50MHz

Serial Data Link Rates:
Remote Serial Port Data Rate - 2.5 Mbits/s
MIL 1553 Data Rate - 1Mbits/s
L2 Transmission Rate - 160 Mbits/s
L3 Transmission Rate - 160 Mbits/s
Encoded Timing Data Rate - 106 Mbits/s

Timing Generator:

Beam Delay Range/Resolution - 600/19 ns
Pipeline Delay Range/Resolution - 4802/19 ns

Test Pulse Delay Resolution - 2ns
Test Pulse Prescale Range - 1 to 65535

Internal Trigger Delay Range/Resolution - 4802/19 ns

DSP Memory Map

Address(Hex)	Device	No. of Bits
0-1FFF	Internal RAM	24
10000-13FFF	Dual Port RAM	16
14000	L1 Crossing Latch	8
14001	L2 Crossing FIFO	9
14002	Internal Crossing Counter	8
14003	Internal Turn Counter	16
14004	L2 Control Word	9
14005	L3 Data Word	16
14006	Hot Link Control Register	8
18000-1FFFF	External System RAM	24
20000-40000	Boot FRAM	8
Flag Out 0	Busy 1	1
Flag Out 1	Busy 2	1
Flag Out 2	Err 1	1
Flag Out 3	Err 2	1

Flag In 0	Init	1
Flag In 1	L2 Decision FIFO Empty	1

Power Consumption (estimated):

+5D: 5A
-5D: 0.5A
+5A, -5A: < 0.1mA

Mechanical:
9U x 280 mm

Front Panel Connectors and Switches:

1 50 pin ribbon cable standard density connector to MRC including:

XING<7:0>	To SRC	Crossing number corresponding to simultaneous assertion of L1ACC, L2ACC, or L2REJ
INIT	To SRC	TFW INIT
L1ACC	To SRC	Level 1 Accept
L2ACC	To SRC	Level 2 Accept
L2REJ	To SRC	Level 2 Reject
TxDAT	To SRC	Serial Data Input
DONE	To SRC	Done processing L3 Data of current event, ready for L3 Data of next event
STRB	To SRC	Strobe for XING<7:0>, L1ACC, L2ACC, & L2REJ
RxDAT	To MRC	Serial Data Output
ERR1	To MRC	Level 1 Error
BUSY1	To MRC	Level 1 Busy, SRC cannot execute L1 Accept
ERR2	To MRC	Level 2 Error
BUSY2	To MRC	Level 2 Busy, SRC cannot execute L2 Accept

1 8 Ribbon Coaxial Connector used differentially including:
  Encoded Beam Timing (106 MHz)
  RF Reference (53MHz)
  L3 Data (160 MHz)
  L2 Data (160 MHz)
1 9 pin “D” connector for the local terminal port
2 Trompeter Tri-Axial Connectors for the MIL 1553 Connection
1 Lemo connector for local trigger out
1 Lemo connector for local trigger in
1 System Reset Switch

Front Panel LEDs:
+5D,-5D,+5A,-5A power indicators
MIL 1553 Remote Terminal Access
MIL 1553 Remote Terminal Timeout